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Huang

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(54) **HIGH VOLTAGE DEVICE WITH
ADDITIONAL ISOLATION REGION UNDER
GATE AND MANUFACTURING METHOD
THEREOF**

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CPC **H01L 29/42368** (2013.01); **H01L 29/0653**
(2013.01); **H01L 29/0696** (2013.01)

(58) **Field of Classification Search**
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USPC 257/337, 339, E29.256, E21.417;
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See application file for complete search history.

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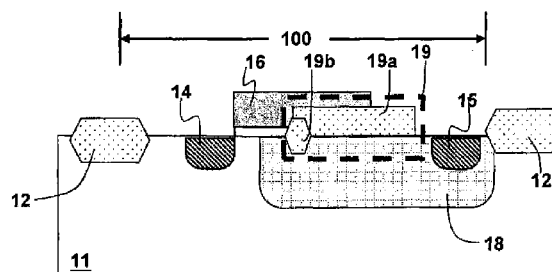
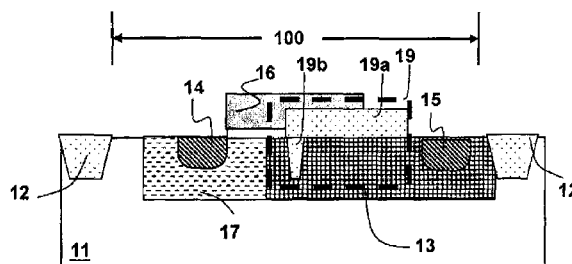
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(57) **ABSTRACT**

A high voltage device includes: a substrate having a first isolation structure to define a device region; a source and a drain in the device region; a gate on the substrate and between the source and the drain; and a second isolation structure. The second isolation structure includes a first isolation region and a second isolation region. The first isolation region is on the substrate and between the source and the drain, and is partially or totally covered by the gate. The second isolation region is in the substrate and below the gate, and has a depth in the substrate which is deeper than the depth of the first isolation region in the substrate, and the length of the second isolation region in a direction along an imaginary line connecting the source and the drain does not exceed one-third length of the first isolation region.

6 Claims, 3 Drawing Sheets



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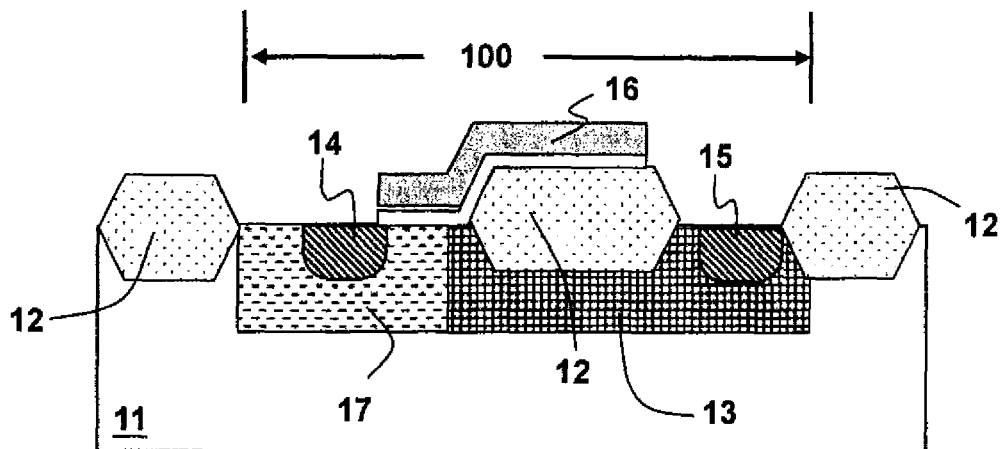


Fig. 1A (Prior Art)

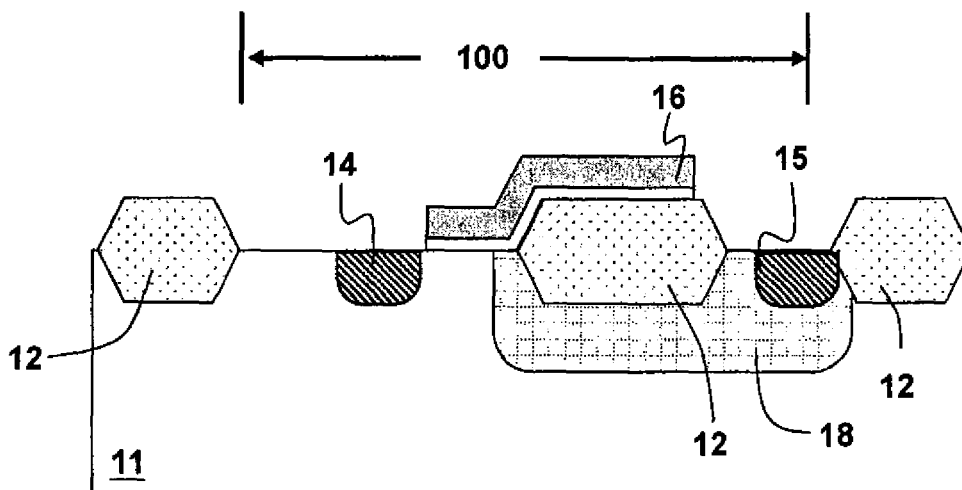


Fig. 1B (Prior Art)

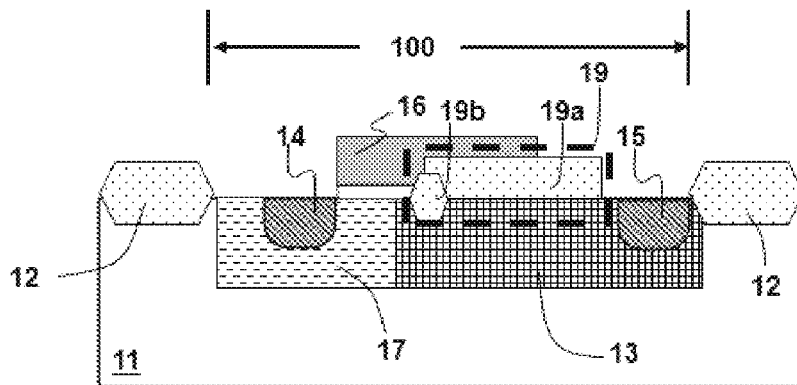


Fig. 2A

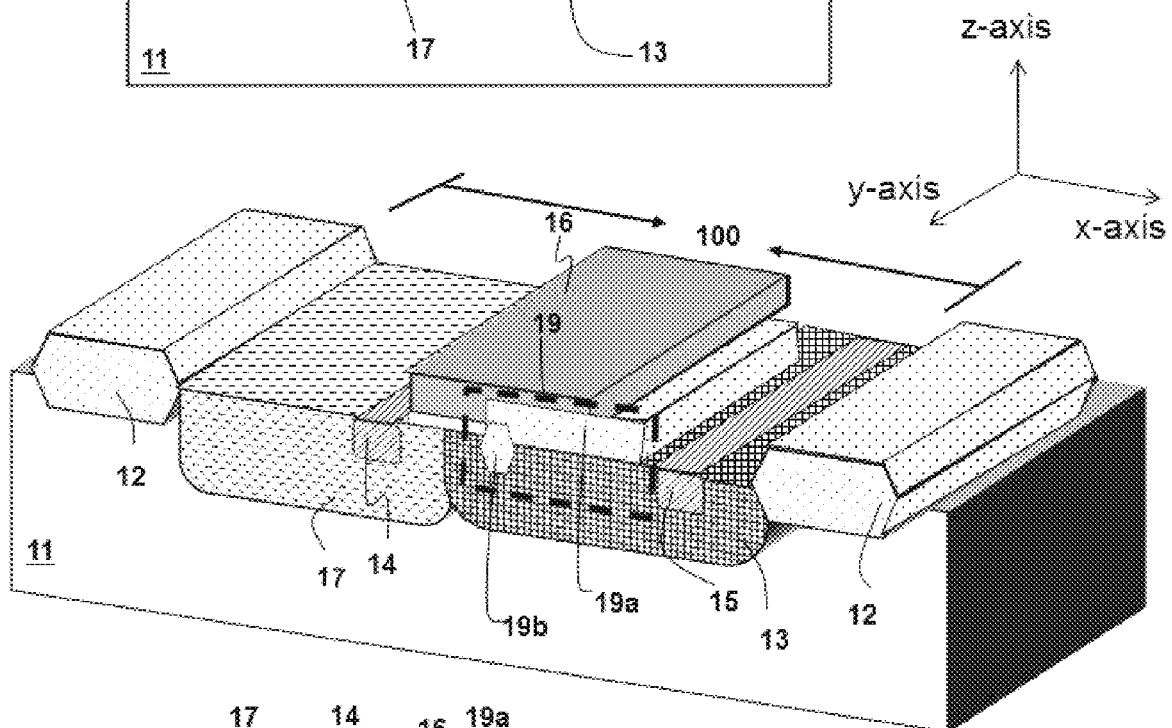


Fig. 2B

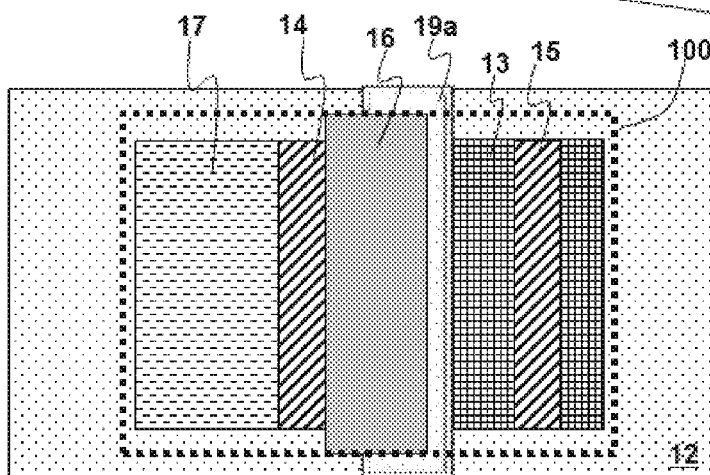


Fig. 2C

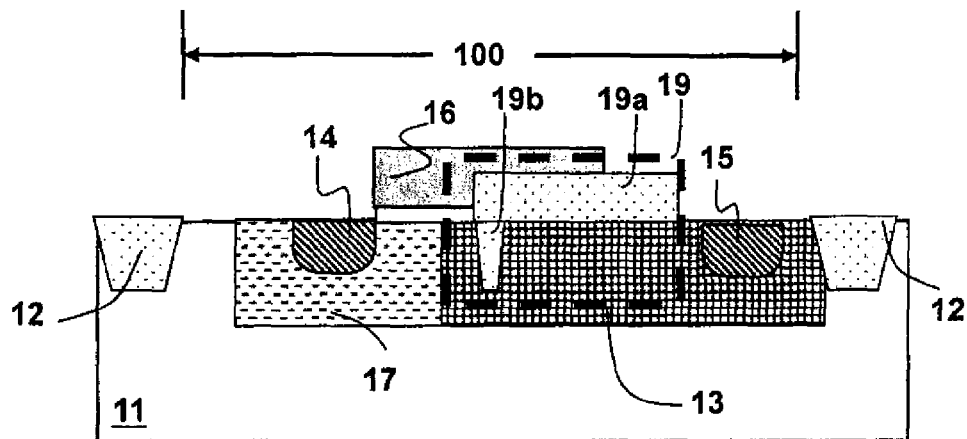


Fig. 3

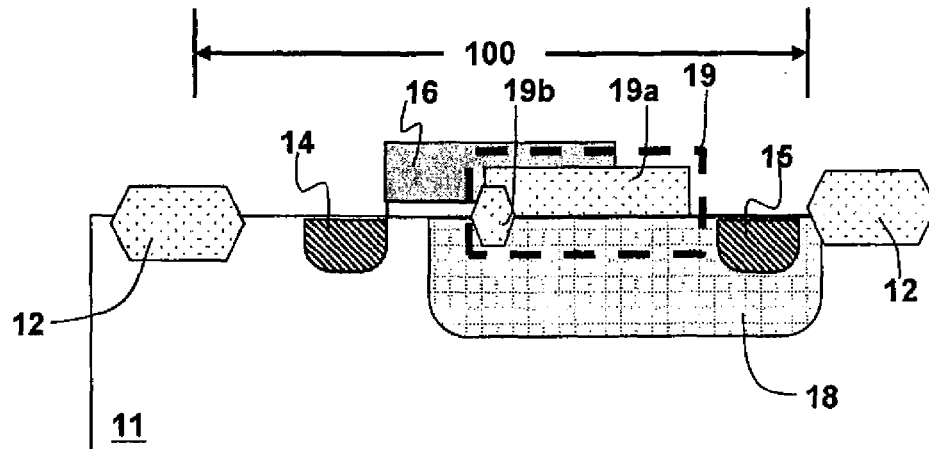


Fig. 4

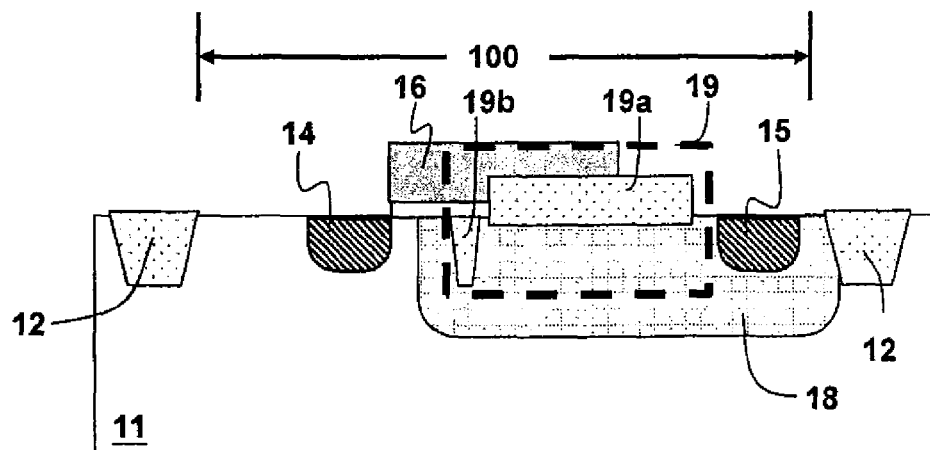


Fig. 5

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HIGH VOLTAGE DEVICE WITH ADDITIONAL ISOLATION REGION UNDER GATE AND MANUFACTURING METHOD THEREOF

BACKGROUND OF THE INVENTION

1. Field of Invention

The present invention relates to a high voltage device and a manufacturing method thereof, in particular to such device with reduced on-resistance and a method for manufacturing the device.

2. Description of Related Art

FIG. 1A shows a cross-section view of a prior art double diffused metal oxide semiconductor (DMOS) device which includes: a P-type silicon substrate **11**; a first isolation structure **12** defining a device region **100**, wherein the isolation structure **12** is formed by, for example, local oxidation of silicon (LOCOS); an N-type well **13** in the substrate **11**; a source **14** and a drain **15** in the device region **100**; a gate **16** between the source **14** and the drain **15**; and a body region **17**. FIG. 1B shows a cross-section view of a lateral double diffused metal oxide semiconductor (LDMOS) device which includes: a P-type silicon substrate **11**; a first isolation structure **12** defining the device region **100**, wherein the isolation structure **12** is formed by, for example, LOCOS; a source **14** and a drain **15** in the device region **100**; a gate **16** between the source **14** and the drain **15**; and a lateral diffusion drain **18** surrounding the drain **15** and separating the source **14** from the drain **15**. Compared with low voltage devices, the prior art high voltage devices have a higher on-resistance (Ron); therefore, in applications requiring high-speed operation, the prior art high voltage devices are less effective.

In view of above, the present invention proposes a high voltage device with reduced Ron and a manufacturing method thereof to overcome the drawback in the prior art, so that the device is more effective in high-speed applications.

SUMMARY OF THE INVENTION

An objective of the present invention is to provide a high voltage device and its manufacturing method.

To achieve the foregoing objective, the present invention provides a high voltage device, comprising: a substrate having a first isolation structure to define a device region; a first conductive type source and a first conductive type drain in the device region; a gate on the substrate and between the source and the drain; and a second isolation structure including: a first isolation region on the substrate and between the source and the drain, wherein from top view, the first isolation region is partially or totally covered by the gate; and a second isolation region in the substrate and below the gate, wherein the second isolation region has a depth in the substrate which is deeper than the depth of the first isolation region in the substrate, and the length of the second isolation region in a direction along an imaginary line connecting the source and the drain does not exceed one-third length of the first isolation region.

The foregoing high voltage device may further include: a second conductive type well surrounding the drain, and a body region surrounding the source, such that the high voltage device forms a DMOS device.

The foregoing high voltage device may further include: a lateral diffusion drain separating the source and the drain, such that the high voltage device forms an LDMOS device.

In the foregoing high voltage device, the second isolation region may be a LOCOS or STI structure.

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In another perspective of the present invention, it provides a method for manufacturing a high voltage device, comprising: providing a substrate; forming a first isolation structure in the substrate to define a device region, and forming a lower isolation region; forming an upper isolation region, wherein the upper isolation region has a depth in the substrate which is smaller than the depth of the lower isolation region in the substrate; forming a gate on the substrate, the gate partially or totally covering the upper isolation region; forming a first conductive type source and a first conductive type drain respectively at the both sides of the gate; wherein the length of the lower isolation region in a direction along an imaginary line connecting the source and the drain does not exceed one-third length of the upper isolation region.

In the foregoing method, the upper isolation region may be formed by depositing isolation material on the substrate, or the upper isolation region and the lower isolation region may be formed at least partially by a same process step.

The objectives, technical details, features, and effects of the present invention will be better understood with regard to the detailed description of the embodiments below, with reference to the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A shows, by cross-section view, a prior art DMOS device.

FIG. 1B shows, by cross-section view, a prior art LDMOS device.

FIGS. 2A-2C show a first embodiment according to the present invention.

FIG. 3 shows a second embodiment according to the present invention.

FIG. 4 shows a third embodiment according to the present invention.

FIG. 5 shows a fourth embodiment according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

The drawings as referred to throughout the description of the present invention are for illustration only, to show the interrelations between the regions and the process steps, but not drawn according to actual scale.

Please refer to FIGS. 2A-2C for a first embodiment of the present invention. FIGS. 2A, 2B, and 2C respectively show, by cross-section view, 3D view, and top view, a DMOS device of the first embodiment according to the present invention, wherein the device includes: a substrate **11** having a first isolation structure **12** to define a first device region **100**; a first conductive type well **13**, a source **14** and a drain **15** in the first device region **100** in the substrate **11**; a gate **16** on the substrate **11**, in the device region **100**, and between the source **14** and the drain **15**; a body region **17** surrounding the source **14**; and a second isolation structure **19**, including: a first isolation region **19a** on the substrate **11**, and between the source **14** and the drain **15**, wherein from top view, the first isolation region **19a**, for example, is partially or totally covered by the gate **16**; and a second isolation region **19b** in the substrate **11**, below the gate **16**, and for example, is located closer to a side of the first isolation region **19a** closer to the source **14** than to a side of the first isolation region **19a** closer to the drain **15**, wherein from top view, the second isolation region **19b**, for example, is partially or totally overlapped by the first isolation region **19a** (in other embodiments, the second isolation region **19b** may alternatively not be overlapped by the first isolation

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region 19a at all), and the length of the second isolation region 19b in x-axis direction (in a direction along an imaginary line connecting the source 14 and the drain 15) preferably does not exceed one-third length of the first isolation region 19a. It should be explained that the wording “the first isolation region 19a on the substrate 11” does not mean that the first isolation region 19a should be completely above the surface of the substrate 11, but means that the first isolation region 19a has a depth in the substrate 11 which is smaller than the depth of the second isolation region 19b in the substrate 11 (therefore, the first isolation region 19a is also referred to as the upper isolation region, and the second isolation region 19b is also referred to as the lower isolation region). Unlike the prior art, the present invention provides the second isolation structure 19 which is different to the conventional first isolation structure 12. In the present invention, at least a large part of the second isolation structure 19 is above the substrate 11, that is, only the second isolation region 19b is substantially in the substrate 11. The second isolation region 19b can suppress the hot carrier effect that degrades the device performance; that is, the second isolation region 19b can suppress the current leakage between the gate 16 and the substrate 11 so that the present invention provides substantially the same advantage as in the prior art, while because at least a large part of the second isolation structure 19 is above the substrate 11, the present invention also reduces Ron so that the device can operate in high-speed and provide a broader range of applications.

Please refer to FIGS. 2A-2C for the manufacturing process steps of the first embodiment according to the present invention. First, the substrate 11 is provided, in which is formed the first isolation structure 12 to define the device region 100, wherein the substrate 11 is, for example, a silicon on insulator (SOI) substrate or a silicon substrate, and the first isolation structure 12 is, for example, a LOCOS structure. Second, the second isolation region 19b can be formed by, for example, the same manufacturing process steps as the first isolation structure 12. Next, the first isolation region 19a can be formed by, for example, depositing isolation material on the substrate 11, or by the same manufacturing process steps as the second isolation region 19b. Next, the first conductive type well 13 is formed by doping first conductive type impurities which may be, for example but not limited to, N-type impurities. Next, the gate 16 is formed. Next, with a mask defined by lithography and the gate 16, an ion implantation process is performed to form a body region 17 with second conductive type impurities which may be, for example but not limited to, P-type impurities. Next, another mask is defined by lithography and the gate 16, and another ion implantation process is performed in the device region 100 to form the source 14 and the drain 15 with the first conductive type impurities which may be, for example but not limited to, the N-type impurities.

FIG. 3 shows a DMOS device of a second embodiment according to the present invention. The structure and manufacturing process steps in this embodiment are similar to those in the first embodiment except the first isolation structure 12 and the second isolation region 19b. In this embodiment, the first isolation structure 12 is an STI structure and the second isolation region 19b is also an STI structure.

FIG. 4 shows an LDMOS device of a third embodiment according to the present invention. Unlike the first embodiment, this embodiment does not have the first conductive type well 13 and the body region 17, but has a lateral diffusion drain 18 separating the source 14 and the drain 15, such that the device becomes the LDMOS device.

FIG. 5 shows an LDMOS device of a fourth embodiment according to the present invention. This embodiment is simi-

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lar to the third embodiment except modifications in the first isolation region 19a and the second isolation region 19b. In this embodiment, the second isolation region 19b is an STI structure, and the first isolation region 19a is not completely above the surface of the substrate 11 but has a little depth in the substrate 11. In addition, the first isolation region 19a does not overlap the second isolation region 19b at all, as shown in the figure.

The present invention has been described in considerable detail with reference to certain preferred embodiments thereof. It should be understood that the description is for illustrative purpose, not for limiting the scope of the present invention. Those skilled in this art can readily conceive variations and modifications within the spirit of the present invention. For example, other manufacturing process steps or structures which do not affect the characteristics of the devices, such as a deep-well region, etc., can be added. As another example, the lithography is not limited to photolithography; it can be electron beam lithography, X-ray lithography or other methods. Further, the number of the second isolation region 19b is not limited to one, but can be multiple. As another example, the second isolation region 19b is not limited to having a uniform thickness as shown in the embodiments, but can have an uneven thickness. Thus, the present invention should cover all such and other modifications and variations, which should be interpreted to fall within the scope of the following claims and their equivalents.

What is claimed is:

1. A method for manufacturing high voltage device, comprising:

providing a substrate having an upper surface;
forming a first isolation structure in the substrate to define a device region, and forming a lower isolation region, wherein the first isolation structure and the lower isolation region are formed by the same process steps, wherein by forming the first isolation structure and the lower isolation region in the substrate, the upper surface of the substrate has recessed portions interfacing the first isolation structure and the lower isolation region, and a flat portion which does not interface the first isolation structure and the lower isolation region;

forming an upper isolation region by depositing an isolation material on the flat portion of the upper surface of the substrate, such that the upper isolation region consists of the isolation material on the flat portion of the upper surface of the substrate;

forming a gate on the substrate, the gate partially or totally covering the upper isolation region; and

forming a first conductive type source and a first conductive type drain respectively at both sides of the gate; wherein the length of the lower isolation region in a direction along an imaginary line connecting the source and the drain does not exceed one-third length of the upper isolation region.

2. The method of claim 1, further comprising: forming a first conductive type well surrounding the drain and a body region surrounding the source, to form a DMOS device.

3. The method of claim 1, further comprising: forming a lateral diffusion drain separating the source and the drain, to form an LDMOS device.

4. The method of claim 1, wherein lower isolation region is a LOCOS structure or an STI structure.

5. The method of claim 1, wherein the lower isolation region is below the upper isolation region and is closer to a side of the upper isolation region closer to the source than to a side of the upper isolation region closer to the drain, and

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wherein from top view, the lower isolation region is partially or totally overlapped by the upper isolation region.

6. The method of claim **1**, wherein the upper isolation region and the lower isolation region are formed at least partially by a same process step.

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